IN THE CLAIMS:

Please amend the pending claim(s) as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (Previously Presented) A controllable amplifier arrangement comprising:

a first differential amplifier stage having a first and a second output branch;

a second differential amplifier stage that is coupled to the first output branch of the first differential amplifier stage, the second differential amplifier stage having a first output branch and at least a second output branch for controllably dividing a first current in the first output branch of the first differential amplifier stage into partial currents, the second output branch having at least one sub-branch that is connected to a current power supply terminal;

a third differential amplifier stage that is coupled to the second output branch of the first differential amplifier stage, the third differential amplifier stage having a first output branch and at least a second output branch for controllably dividing a second current in the second output branch of the first differential amplifier stage into partial currents, the second output branch having at least one sub-branch that is connected to a current power supply terminal;

a first load impedance coupled to one of the output branches of the second differential amplifier stage for generating a first output voltage from the partial current flowing in said one of the first output branches of the second differential amplifier stage; and

a second load impedance coupled to one of the output branches of the third differential amplifier stage for generating a second output voltage from the partial current flowing in said one of the first output branches of the third differential amplifier stage;

wherein the first and the second load impedance are bridged to a predetermined part by at least one of the second output branches of the second and third differential amplifier stages, respectively.

2. (Previously Presented) The controllable amplifier arrangement as claimed in claim 1, wherein said one of the second output branches of the second differential amplifier stage has two jointly controlled sub-branches, a first sub-branch of which is coupled to the first load impedance, and wherein said one of the second output branches of the third differential amplifier stage has two jointly controlled sub-branches, a first sub-branch of which is coupled to the second load impedance.

3. (Previously Presented) The controllable amplifier arrangement as claimed in claim 1, wherein said one of the second output branches of the second differential amplifier stage is coupled to a tap on the first load impedance, and said one of the second output branches of the third differential amplifier stage is coupled to a tap on the second load impedance.

4. (Currently Amended) An arrangement for processing electric signals, comprising at least one controllable amplifier arrangement, the controllable amplifier comprising:

a first differential amplifier stage having a first and a second output branch;

a second differential amplifier stage that is coupled to the first output branch of the first differential amplifier stage , the second differential amplifier stage having a first output branch and at least a second output branch for controllably dividing a first current in the first output branch of the first differential amplifier stage into partial currents, the second output branch having at least one sub-branch that is connected to a current power supply terminal;

a third differential amplifier stage that is coupled to the second output branch of the first differential amplifier stage, the third differential amplifier stage having a first output branch and at least a second output branch for controllably dividing a second current in the second output branch of the first differential amplifier stage into partial currents, the second output branch having at least one sub-branch that is connected to a current power supply terminal;

a first load impedance coupled at a first terminal to ~~one of~~ the first output branches of the second differential amplifier stage and coupled at a second terminal to at least one sub-branch of the second output branch of the second differential amplifier stage for generating a first output voltage from the partial current flowing in said one of the first output branches of the second differential amplifier stage; and

a second load impedance coupled at a first terminal to ~~one of~~ the first output branches of the third differential amplifier stage and coupled at a second terminal to at least one sub-branch of the second output branch of the third differential amplifier stage for generating a second output voltage from the partial current flowing in said one of the first output branches of the third differential amplifier stage.

5. (Previously Presented) The arrangement for processing electric signals as claimed in claim 4, comprising at least two controllable amplifier arrangements, wherein the second and the third differential amplifier stage of the controllable amplifier arrangements are controllable by means of common control signals and have control characteristics which are mutually offset in such a way that the partial currents flowing in the output branches of the second and the third differential amplifier stage are reversed in the individual controllable amplifier arrangements at different values of the common control signals.

6. (Previously Presented) The arrangement for processing electric signals as claimed in claim 5, wherein the output branches of the second and the third differential amplifier stage are formed with transistors whose main current paths have current conveying cross-sectional areas whose dimensioning determines the reversal of the partial currents in the output branches of the second and third differential amplifier stages of the individual controllable amplifier arrangements at the different values of the common control signals in the individual controllable amplifier arrangements.

7. (Previously Presented) The controllable amplifier arrangement of claim 1, wherein the first amplifier differential stage comprises a plurality of bipolar transistors.

8. (Previously Presented) The controllable amplifier arrangement of claim 7, wherein the second amplifier differential stage comprises a plurality of bipolar transistors.

9. (Previously Presented) The controllable amplifier arrangement of claim 1, wherein the first load impedance is an ohmic resistor.

10. (Currently Amended) The arrangement for processing electric signals of claim 4, wherein said one of the second output branches of the second differential amplifier stage has two jointly controlled sub-branches, a first sub-branch of which is coupled to the first load impedance, and wherein~~in that~~ said one of the second output branches of the third differential amplifier stage has two jointly controlled sub-branches, a first sub-branch of which is coupled to the second load impedance.

11. (Previously Presented) The arrangement for processing electric signals as claimed in claim 10, comprising at least two controllable amplifier arrangements, wherein the second and the third differential amplifier stage of the controllable amplifier arrangements are controllable by means of common control signals and have control characteristics which are mutually offset in such a way that the partial currents flowing in the output branches of the second and the third differential amplifier stage are reversed in the individual controllable amplifier arrangements at different values of the common control signals.

12. (Previously Presented) The arrangement for processing electric signals as claimed in claim 11, wherein the output branches of the second and the third differential amplifier stage are

formed with transistors whose main current paths have current conveying cross-sectional areas whose dimensioning determines the reversal of the partial currents in the output branches of the second and third differential amplifier stages of the individual controllable amplifier arrangements at the different values of the common control signals in the individual controllable amplifier arrangements.

13. (Previously Presented) The arrangement for processing electric signals of claim 4, wherein said one of the second output branches of the second differential amplifier stage is coupled to a tap on the first load impedance, and said one of the second output branches of the third differential amplifier stage is coupled to a tap on the second load impedance.

14. (Previously Presented) The arrangement for processing electric signals as claimed in claim 13, comprising at least two controllable amplifier arrangements, wherein the second and the third differential amplifier stage of the controllable amplifier arrangements are controllable by means of common control signals and have control characteristics which are mutually offset in such a way that the partial currents flowing in the output branches of the second and the third differential amplifier stage are reversed in the individual controllable amplifier arrangements at different values of the common control signals.

15. (Previously Presented) The arrangement for processing electric signals as claimed in claim 14, wherein the output branches of the second and the third differential amplifier stage are formed with transistors whose main current paths have current conveying cross-sectional areas whose dimensioning determines the reversal of the partial currents in the output branches of the second and third differential amplifier stages of the individual controllable amplifier arrangements at the different values of the common control signals in the individual controllable amplifier arrangements.

16. (Previously Presented) The arrangement for processing electric signals as claimed in claim 13, wherein the first differential amplifier stage comprises a plurality of bipolar transistors.

17. (Previously Presented) A controllable amplifier, comprising:

a first-stage differential amplifier having a first and a second output branch;

a second-stage differential amplifier coupled to the first first-stage output branch, the second-stage differential amplifier having a first and a second output branch for controllably dividing a first current in the first first-stage output into partial currents;

a third-stage differential amplifier coupled to the second first-stage output branch, the third-stage differential amplifier having a first and a second output branch for controllably dividing a first current in the second first-stage output into partial currents;

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a first second-stage impedance load coupled to the first second-stage output branch;

a second second-stage impedance load coupled to the first second-stage impedance load and to the second second-stage output branch, and connected to a current power supply terminal, the first and second second-stage impedance loads for generating a first output voltage at an output tap coupled between them;

a first third-stage impedance load coupled to the first third-stage output branch; and

a second third-stage impedance load coupled to the first third-stage impedance load and to the second third-stage output branch, and connected to a current power supply terminal, the first and second third-stage impedance loads for generating a second output voltage at an output tap coupled between them;

wherein the first output branches of the first-stage and the second-stage differential amplifiers are each coupled to be controlled by a first control voltage, and wherein the second output branches of the first-stage and the second-stage differential amplifiers are each coupled to be controlled by a second control voltage.

18. (Previously Presented) The controllable amplifier arrangement of claim 17, wherein the first second-stage impedance load is an ohmic resistor.

19. (Previously Presented) The controllable amplifier arrangement of claim 17, wherein the first-stage differential amplifier comprises a plurality of bipolar transistors.

20. (Previously Presented) The controllable amplifier arrangement of claim 19, wherein the second-stage differential amplifier comprises a plurality of bipolar transistors.